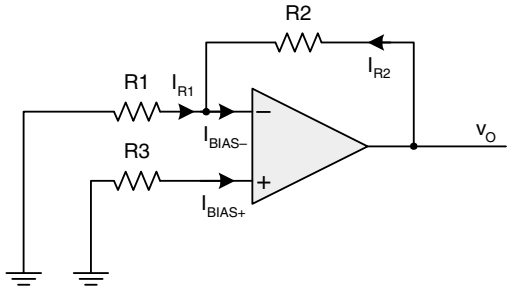


**FIGURE 14.11** Mitigating $I_{BIAS}$ with matched input resistor.

$I_{BIAS+}$ now causes a voltage drop across $R3$, which is reflected at the negative terminal by reason of the virtual short. $V_- = V_+ = 0 - I_{BIAS+}R3$. Therefore, the current through $R1$ is $I_{R1} = I_{BIAS+}R3 \div R1$. The currents flowing through $R1$ and $R2$ into the negative terminal must equal $I_{BIAS-}$, because current does not simply disappear. Per node analysis, the sum of the currents entering a node must equal the sum of the currents leaving that node. This relationship can be restated to solve for the current through $R2$.

$$I_{R2} = I_{BIAS-} - I_{R1} = I_{BIAS-} - I_{BIAS+}\frac{R3}{R1}$$

Knowing $I_{R2}$ enables the final expression of the output voltage,

$$V_O = V_- + I_{R2}R2 = (-I_{BIAS+})R3 + \left[I_{BIAS-} - I_{BIAS+}\frac{R3}{R1}\right]R2$$

By temporarily assuming that $I_{IO} = 0$, $I_{BIAS+} = I_{BIAS-}$. This reduces the output voltage expression to

$$V_O = I_{BIAS}\left[-R3 + R2 - \frac{R2R3}{R1}\right] = I_{BIAS}\left[R2 - R3\left(1 + \frac{R2}{R1}\right)\right]$$

This expression shows that the effects of $I_{BIAS}$ can be compensated for by choosing $R3$ such that $V_O = 0$. Solving for $R3$ when $V_O = 0$ yields the parallel combination of $R1$ and $R2$,

$$R3 = \frac{R2}{1 + \frac{R2}{R1}} = \frac{R1R2}{R1 + R2}$$

A similar compensation can be designed for the case of an AC-coupled circuit, but it differs by taking into account the fact that no current flows through the coupling capacitor at DC. The circuit in Fig. 14.9 can be augmented by adding a resistor to the positive input terminal as shown in Fig. 14.12.

Unlike in the previous DC circuit, all of $I_{BIAS-}$ flows through the feedback resistor, and the output voltage is

$$V_O = V_- + I_{BIAS-}R2 = V_+ + I_{BIAS-}R2 = -I_{BIAS+}R3 + I_{BIAS-}R2$$

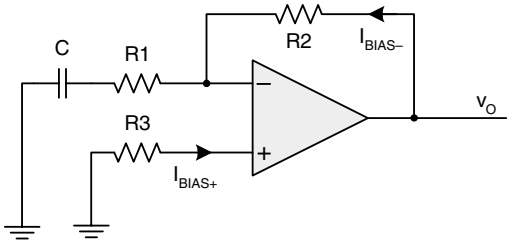


**FIGURE 14.12** Mitigating $I_{BIAS}$ in an AC coupled circuit.

If the input bias currents are assumed to be equal, selecting $R3 = R2$ nulls out the effects of $I_{BIAS}$ in the AC coupled circuit.

Unfortunately, $I_{IO}$ remains a problem in both the DC and AC circuits, although it is a problem of less magnitude than that of uncompensated $I_{BIAS}$. In Fig. 14.10, it was observed that uncompensated $I_{BIAS}$ results in $V_O = I_{BIAS}R2$. Once $I_{BIAS}$ has been compensated for by the inclusion of a resistor in the positive input terminal, $I_{IO}$ effectively becomes the uncompensated $I_{BIAS}$ term, resulting in $V_O = I_{IO}R2$. Again, $I_{IO}$ as specified in nanoamps and picoamps may not present much problem for many circuits in which the feedback resistor, $R2$, is relatively small.

Continuing down the LM741 data sheet, additional physical realities are observed. Input voltage levels are limited by the chip's supply voltages. As the input levels approach the supply voltages, the op-amp's ability to deliver ideal performance diminishes. Supply voltages also relate to the output voltage swing of the op-amp. Many op-amps are unable to drive *rail-to-rail*. In other words, if an op-amp's supply voltages are ±15 V, the range of output voltages may be only ±14 V under lightly loaded conditions (10 kΩ in the LM741's case). As the output current demand increases, the op-amp's guaranteed drive level is diminished. Modern op-amps are available with a wide range of output drive strengths and characteristics. Rail-to-rail op-amps guarantee the ability to drive to within millivolts of either voltage supply at their rated drive current.

An op-amp is a differential amplifier with an ideal transfer function of $v_O = Av_D$. According to this simple relationship, only the voltage difference between the positive and negative terminals has any bearing on the output voltage. The same $v_D$ results when $v_+ = 0.02$ V and $v_- = 0.01$ V as when $v_+ = 10.02$ V and $v_- = 10.01$ V. Ideally, the *common-mode* voltage, that voltage applied to both terminals, has no effect upon the output voltage. The first and second pairs of input levels have common-mode voltages, $v_{CM}$, of 0.01 and 10.01 V, respectively. Both pairs of inputs may be within the specified input range of a particular op-amp, but each pair will cause somewhat different behavior. The reason for this is that a real op-amp does not contain a perfect differential amplifier. The internal amplifier has some sensitivity to the common-mode signal that is applied to it.

If the inputs of an op-amp are tied together and a common-mode voltage is applied, there will be some nonzero output response even if the circuit has already been compensated for input offset errors. An op-amp has a finite common-mode gain associated with it such that $v_O = A_{CM}v_{CM}$ independent of the differential gain, $A$. Manufacturers define a *common-mode rejection ratio* (CMRR) that specifies the ratio of differential to common mode gain,

$$CMRR = 20\log\frac{A}{A_{CM}}$$

CMRR is expressed in decibels to more easily represent large ratios. A high CMRR indicates that $A >> A_{CM}$, which means that undesired effects due to common-mode input voltages are reduced.